

1 ASYNCHRONOUS TRANSFER MODE, filed 10/02/2000; Patent
2 Application Serial No. 09/964,158 (TI-33430), titled
3 APPARTUS AND METHOD FOR AN INTERFACE UNIT FOR DATA TRANSFER
4 BETWEEN A HOST PROCESSING AND A MULTI-TARGET DIGITAL SIGNAL
5 PROCESSING IN AN ASYNCHRONOUS TRANSFER MODE, filed
6 09/26/2001; Patent Application Serial No. 09/964,159
7 (TI-33534), titled APPARATUS AND METHOD FOR AN INTERFACE
8 UNIT FOR DATA TRANSFER BETWEEN DATA PROCESSING UNITS IN THE
9 ASYNCHRONOUS TRANSFER MODE AND IN THE I/O MODE, filed
10 09/26/2001; and Patent Application Serial No. 09/964,164
11 (TI-33533), titled APPARATUS AND METHOD FOR INPUT CLOCK
12 SIGNAL DETECTION IN AN ASYNCHRONOUS TRANSFER MODE INTERFACE
13 UNIT, filed 09/26/2001."

14

15 **Remarks**

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17 Claims 1-17 have been presented for examination in the
18 above identified U.S. Patent Application.

19

20 Claims 1-17 have been rejected in the above-identified
21 Office Action.

22

23 Claims 1, 3, 5, 6, 10, 13, 14, and 17 have been
24 amended by this Amendment A.

25

26 Claims 9 and 15 have been canceled by this Amendment
27 A.

28

1 Claims 1-8, 10-14, 16 and 17 are still in the
2 Application and reconsideration of the application is
3 hereby respectfully requested.
4

5 Referring to Paragraph 1 of the Office Action, the
6 specification has been objected to because of cited
7 informalities. The informalities cited by Examiner have
8 been corrected by this Amendment A. Therefore, the
9 objections to the informalities in the Specification have
10 been answered by amendment.
11

12 Referring to Paragraph 2 of the Office Action, Claims
13 1 and 5 have been objected to because of cited
14 informalities. The informalities cited by Examiner have
15 been corrected by this Amendment A. Therefore, objection
16 to Claims 1 and 5 because of the cited informalities have
17 been answered by amendment.
18

19 Referring to Paragraph 3 of the Office Action, Claims
20 1-3, 7, 8, 14 and 16 have been rejected under 35 U.S.C.
21 102(b) as being anticipated by U.S. Patent 6,732,206 issued
22 in the name of Jensen et al (hereinafter referred to as
23 Jensen). Referring to Paragraph 4 of the Office Action,
24 Claims 4 and 17 have been rejected under 35 U.S.C. 103(a)
25 as being unpatentable over Jensen in view of U.S. Patent
26 5,941,952 issued in the name of Thomas et al (hereinafter
27 referred to as Thomas. Claims 5, 6, 9, 10, 12, 13, and 15
28 have been rejected under 35 U.S.C. 103(a) as being
29 unpatentable over Jensen in view of U.S. Patent 6,732,206

1 issued on the name of Kessler et al (hereinafter referred
2 to as Kessler.

3
4 Claims 1, 10 and 14, the independent claims of the
5 Application have been amended to include the limitation
6 that the slave processor includes a direct memory access
7 unit. This limitation is specifically shown in Fig. 5 of
8 the Application and discussed in the specification. A
9 plurality of (slave) digital signal processing units is
10 fabricated on a signal chip and a direct memory access unit
11 is also provided to distribute the incoming data cells to
12 the correct location. The present invention is a simple
13 interface unit that does not require a complete reworking
14 of the already-designed direct memory access unit. In
15 addition to the minimum redesign effort to accommodate the
16 UTOPIA format, the presence of this limitation is important
17 for the following reason. In the ATM mode of operation,
18 the rate of data transfer over the communication bus is
19 much slower than the rate of data flow needed by the
20 central processing unit. The interface unit and the direct
21 memory access unit provide a buffer between the
22 communication bus and the processing unit. For the
23 processing systems contemplated by the present application,
24 the direct memory access unit participates in the buffering
25 and places different requirements on the processing
26 capability. The processing systems envisioned by the
27 present invention include a master data processing unit, a
28 communication system an interface unit, a direct memory
29 access unit, and a plurality of slave processing unit. The
30 present invention specifically involves the interface unit.

1 The interface unit of the present invention serves the
2 function of buffering between rate of data transfer on the
3 communication bus and the rate of data transfer in the
4 direct memory access unit and translating the address with
5 the incoming data cells. The incoming address provides the
6 slave data processing memory location to which the data
7 cell is directed.

8

9 With particular reference to the Jensen reference,
10 note that in claim 1, the limitation is present that the
11 "slaves having a maximum granularity greater than the
12 maximum number of supported addresses". Claim 10 includes
13 the limitation of "queuing the cell to a port specified by
14 the internal address". And Claim 13 includes the
15 limitation "a queue associated with the port". Thus all of
16 the independent claims of the principal reference have
17 claims limitations that are not found in the Claims of the
18 Application as amended. In addition to the presence of
19 foregoing limitations found in the Claims of the Jensen
20 reference but not in the Claims of the Application, the
21 invention of the Jensen reference requires generation of
22 port addresses and queues, neither of which is found in the
23 interface unit of the present Application.

24

25 Similarly, the Kessler reference and the Thomas
26 reference do not disclose a memory access unit. Instead,
27 the functions performed by the direct memory access unit
28 are specifically designed as part of the interface.
29 Therefore, these references do not disclose, claim, or even
30 suggest the interface unit of the present invention.

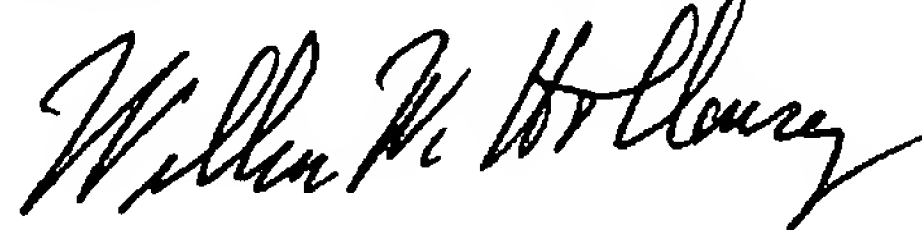
1 Consequently, rejection of the Claims 1-17 under 35
2 U.S.C. 102(b) by reference to Jensen, either alone or in
3 combination with Thomas and Kessler under 35 U.S.C. 103(a),
4 is respectfully traversed.
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2
3 **CONCLUSIONS**

4 In view of the foregoing amendments and the foregoing
5 discussion, it is believed that Claims 1-8, 10-14, 16 and
6 17 are now in condition for allowance and allowance of
7 Claims 1-8, 10-14, 16 and 17 is hereby respectfully
8 requested and the Notice of Allowance be issued in a timely
9 fashion.

10 Should any issues remain that can be resolved by a
11 telephone interview, Examiner is respectfully requested to
12 contact the undersigned attorney at the number listed
13 below.

Respectfully submitted,



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